Testing of Cylindrical Surrounding Double-Gate MOSFET Parameters Using Image Acquisition

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Abstract

In this paper, we have analyzed the image acquisition of the Cylindrical Surrounding Double-Gate (CSDG) MOSFETs for the purpose of RF switch for the advanced wireless telecommunication systems. The proposed model will emphasize on the basics structure of the single image sensor for two dimensional images of a three dimension devices, so that we can obtained a satisfied or say smooth device structure and hence some of its parameter. The physical significance of these basic structure elements are also has been discussed.

Keywords: CMOS image sensors; Cylindrical surrounding double-gate (CSDG) MOSFET; Double-gate (DG) MOSFET; Image acquisition; Image processing; RF switch; VLSI

1. Introduction

An advantage of extremely thin devices is that they do not suffer from the transients, simply because the back interface cannot be driven in accumulation. Since the primary intrinsic variations include the random dopant fluctuation, which is caused by uncertainty in charge location and charge numbers such as the discrete placement of dopant atoms in the channel region that follows the Poisson distribution (Ye and Cao 2010). As the device size scale down, the total number of channel dopants decreases, which provides a larger variation of dopant numbers and significantly impacting the threshold voltage (Kang and Leblebichi 2002; Tang et al. 2010; Srivastava et al. 2011(a)).

The CSDG MOSFET structure (shown in the Fig. 1) utilizes an undoped body because the undoped MOSFET can avoid the dopant fluctuation effect, which contributes to the variation of threshold voltage and switch ON current. So the SCDG MOSFET (Srivastava et al. 2011(b)) can be used for the purpose of Double-Pole Four-Throw (DP4T) RF CMOS switch design (Cheralathan et al. 2011;
Kolberg et al. 2008; Srivastava et al. 2011(c)). However, the undoped body can enhance the carrier mobility owing to the absence of depletion charges which can significantly contributes to the effective electric field, thus degrading the mobility (Cerdeira et al. 2008; Reyboz et al. 2009; Tamer and Roy 2007).

The image processing is frequently used in the systems for monitoring and controlling of objects to help in effective management of their resources, safety, and robots controlling (Dutkiewicz et al. 2010). The practical systems for monitoring Cylindrical objects, like for example CSDG MOSFET which requires various vision sensors for recording the images that have to be transmitted for the processing into the central processing unit. One of the most challenging problems in such cases is effective transmission and processing of a large amount of image details and its equivalent data. To avoid overloading of transmission in transmission channels and in central unit, some early vision algorithms are frequently used at the sensors by an integrated low level image processor. As a result the rough image data, generated by the sensors, can be compressed or replaced by useful information extracted from images. This approach significantly improves the overall efficiency and the cost of a system implementation by relaxing requirements on throughput of transmission channels and demands on processing speed of the central processing unit (Jendernalik et al. 2011). A complete vision chip consisting of a photo-detector array can effectively be implemented in CSDG MOSFET, which is formed on the cylindrical substrate.

Fig 1. Schematic of the (a) CSDG MOSFET and (b) cross-section of CSDG MOSFET (Srivastava et al. 2011(a))
The earlier solutions of integrated chips were mostly dedicated to a specific image algorithm and could not be reconfigured. The next generations of programmable vision chips, designed in single instruction multiple data (SIMD) architectures or multiple instructions multiple data (MIMD), were able to perform several image algorithms (Cummings et al. 2001; Dupret et al. 2002; Martin et al. 1998; Schemmel et al. 2002). The newest chips have fully programmed architectures with a parallel analogue data processing, which significantly reduces the time necessary for an image processing (Dudek and Hicks 2001; Dudek and Hicks 2005). Although, the recent development in vision chip implementations is great, there are still some areas for improvements.

Most of the reported vision chips realize the convolution algorithms, where only four neighboring pixels (the top, bottom, left, and right) are taken into calculations. The consequence of the omitting the other pixels is degradation of the resulting image. Some of the reported implementations (Dudek et al. 2009) have speed limitation resulting from the sequential manner of instruction processing, which means that a typical convolution algorithm requires several clock cycles to calculate single data which increases the processing time.

A recently emerging 3-D integrated technology offers a promising approach to upgrade the applications. In this technology, several Silicon-on-Insulator (SOI) levels with different circuits can be vertically stacked and interconnected through the vias. This high intensity integration topology allows a vision sensor to separate photo sensitive devices with processing circuits on different layers to achieve a high resolution. Recent publications have reported image sensors designed and fabricated using this process (Culurciello and Weerakoon 2007; Suntharalingam et al. 2005). Blakiewicz (2009) proposed a matrix multiplier for an integrated low power and low cost image sensor design as a better alternative to known parallel architectures. The circuit, although less flexible in number of possible to implement algorithms, characterizes very low power consumption and occupied less chip area.

In this paper, we have proposed a model for image acquisition by which we will verify the surface of the CSDG MOSFET means surface of the CSDG MOSFET is smooth or not. If it is smooth then we proceed for the further testing and processing, otherwise device fails. The design of the proposed model has been studied to understand the effect of device geometry useful when working as a switch. Each steps of the model are discussed separately for the purpose of clarity of presentation and understanding the process for the device (CSDG MOSFET). The organization of the paper is as follows. The CSDG MOSFET model is presented in the Section 2. The proposed model for the image acquisition of the device is discussed in the Section 3. Discussions about the model of image acquisitions are summarized in the Section 4. Finally, the Section 5 concludes the work and recommends the future directions.

2. Design of CSDG MOSFET

In a MOSFET, the double-gate provides various performance enhancements such as increased transconductance and a lower threshold voltage. In the DG MOSFET (Srivastava et al. 2011(a)) when voltage is applied to the gates of device, the active silicon region is so thick, such that the control region of the silicon remains controlled by the majority carriers in that region, which develops two channels named as gate $G_1$ and gate $G_2$. One channel forms near the top boundary between the Silicon and Silicon-insulator and the other one form like wise at the bottom interface.
The performance of the symmetrical version of the DG MOSFET is further increased by higher channel mobility compared to the bulk MOSFET, since the average electric field in the channel is lower, which reduces interface roughness scattering according to the universal mobility model (Bigas et al. 2006).

The basic concept of a CSDG MOSFET is to control the Silicon channel very effectively by choosing the Silicon channel width to be very small and by applying a gate contact to both sides of the channel, which is of cylindrical type. This concept helps to suppress the short channel effect (SCE) and leads to higher currents as compared with a MOSFET having only one gate. We have alrady presented 2-D physics based modeling of the short-channel CSDG MOSFETs of the nanoscale dimensions (Srivastava et al. 2013). Due to the circular source and drain, the gate contact with the source and drain are on a long circular region, which avoids the gate misalignment.

3. Proposed model for the Image Acquisition of CSDG MOSFET

The CMOS image sensors are nowadays extensively used in research, scientific, and commercial applications. The CMOS standard processes, which are developed for digital and mixed signal applications, are really attractive particularly because of their low power consumption, applicability for on-chip signal processing and large availability. Various processes have been explored to improve the image sensor performance. These performances have been significantly enhanced with the use of CMOS image sensor processes (Furumiya 2001). In addition, the use of upgraded technologies and smaller MOS transistors (gate area 1 mm$^2$) in the pixel are required in order to maximize the pixel photosensitive area. This leads to an increase of MOS transistor low frequency noise impact (Dudek and Hicks 2000; Gonthier et al. 2010; Gonzalez and Woods 2002; Jutier et al. 1983; Petrou and Bosdogianni 2000).

To measure the parameters of the device we have proposed a model using image acquisition (Andreou et al. 1995) process as shown in the Fig. 2. The details of the process performed in the flow graph are given as below:

3.1 Pre Processing and Image Sensor
First, we put the device on the base of the image sensor to capture the image using the conveyor moving belt. For the proposed model we convert the CSDG MOSFET into the image. For this purpose we have to generate a two dimensional image of the device means sensor should have displacement in X and Y direction between the sensor and the area to which be imaged. A negative film is mounted on the CSDG MOSFET and a mechanical moment of MOSFET provides the displacement in one direction. A sensor is mounted on the lead that provides motion in perpendicular direction (Cheng et al. 1990; Gamal and Eltoukhy 2005; Tan and Buttgen 2010).

3.2 Discrete Fourier Transform
The image obtained from the above image sensor process, there may be some reductions in the property of image e.g. contrast, brightness, sharpness, and colour. To enhance the property of image, we use the process of the Discrete Fourier Transform (DFT) because this transform is an important tool in the area of digital signal processing. Since the DFT requires intensive computation, so there is fast DFT processors to meet real-time signal processing requirements (Chang 2000).
**Fig 2.** Flow chart of a CSDG MOSFET device

- **Pre-Processing**
  - Image Sensor
  - Discrete Fourier Transform
  - Filter Function
  - Inverse Discrete Fourier Transform

- **Post-Processing**
  - Results in form of parameters
  - Results compared with the stored parameters
    - **No**
    - **Yes**
      - Device passes the Testing stage
3.3 Filter Function

We pass the above DFT image through a filter which has the Filter function $H(u, v)$. This filter function is set by the requirement for the image. Smoothing of the image is achieved in the frequency domain by dropping out the high frequency components means using the low pass filter function. Sharpening, enhancing or detecting the edges of the images is associated with high frequency components which can be achieved with the application of high pass filter.

3.4 Inverse Discrete Fourier Transform and Post Processing

Finally, we compute the inverse DFT of the signal obtained from the $F(u, v)$ multiplied by a filter function $H(u, v)$. So, we achieved the enhanced image (Van et al. 2005).

In the post processing step, image is enhanced. The image enhancement is a process that changes the pixel’s intensity of the input image, so that the output image contains all the property of the device under test (DUT). It also enhances the interpretability and perception of information contained in the image. Image enhancement can also be used to provide a better input for other automated image processing systems. One of the commonly used image enhancement methods is histogram equalization (Dudek and Hicks 2000; Gonzalez and Woods 2002). This equalization remaps the gray level of an image based on the probability distribution of the input gray levels. It flattens and stretches the dynamic range of the image’s histogram so this result in an overall contrast enhancement by changing the intensity level of the pixels based on the intensity distribution of the input image.

The sub regions histogram equalization partitions the image based on the smoothed intensity values, which are obtained by convolving the input image with a Gaussian filter. By doing this, the transformation function used by histogram equalization is not based on the intensity of the pixels only, but the intensity values of the neighboring pixels are also taken into the consideration (Corry et al. 1983; Ibrahim and Kong 2009).

4. Discussions

After obtaining the parameter from the post processing, we have compared these parameters with the already stored parameters, which are required by the company or consumer for the device. If comparison of the parameter fails then the process will be repeated, else it passes the parameter comparison and we can achieve the pass device.

In the way of the above processing, we can get the image of a device (CSDG MOSFET) of various types as shown in the Fig. 3. In this figure we can compare the structure of the device. If the image obtained from the post processing stage is different at any stage, we can remove the device and further design can be improved for the suitable structure of the device as to be cylindrical and flatness at the surfaces in this particular stage. So, we can improve the device structure using the image acquisition phenomenon. As here in this work we have taken the cylindrical device (CSDG MOSFET), but this process is also suitable for rectangular and cubical device such as double-gate (DG) MOSFET, FinFET, and Gate all around (GAA) structures.
<table>
<thead>
<tr>
<th>(a) Original Device</th>
<th>(b) Transparent colored</th>
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<tbody>
<tr>
<td><img src="image1" alt="Original Device" /></td>
<td><img src="image2" alt="Transparent colored" /></td>
</tr>
<tr>
<td>(c) Washout</td>
<td>(d) Gray scaled</td>
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<tr>
<td><img src="image3" alt="Washout" /></td>
<td><img src="image4" alt="Gray scaled" /></td>
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<tr>
<td>(e) Black and White</td>
<td>(f) Image Obtained</td>
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<td><img src="image5" alt="Black and White" /></td>
<td><img src="image6" alt="Image Obtained" /></td>
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**Fig 3.** Various images obtained from the Image Acquisition of the CSDG MOSFET

## 5. Conclusion and Future Recommendations

In this paper, we have analyzed the image acquisition of the CSDG MOSFETs for the purpose of RF switch for the advanced wireless telecommunication systems. The proposed model emphasized on the basics of the single image sensor for two dimensional images of a three dimension devices so that we can obtained a satisfactory device parameter. Using this technique we can verify the basics of the circuit elements parameter required for the radio frequency sub-systems of the integrated circuits such as capacitances, resistances, oxide thickness, resistance of poly-Silicon, number of bulk capacitors. The model can be easily introduced into the circuit simulators.
Beyond the proposed model in this work, it has some potential challenges such as the accuracy of the device contact which is a tricky process, which will be reported in the future communications. In the presented work, we apparently restrict the analysis of the spherical devices because it requires a number of image sensors to take the image of device from various angles. As a consequence, the comparisons have been made in regard to the available modes of the image sensor. Above discussed drawbacks can also be taken into account in the future works.

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Biography

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